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# Evaluation Report

**RELIABILITY DEPARTMENT**

STUDY OF FAILURE AND RELIABILITY
IN MICROELECTRONICS DEVICES

2nd Quarterly Report
February 1966

CONTRACT NAS 12-72

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Electronic Research Center

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## 1.0 INTRODUCTION

The present study into the physics of failure of microelectronic devices is being undertaken to obtain results that will lead to better definition and specification of modes of failure and failure rates.

The basic objective of the program is defined to:

1) determine basic failure mechanisms and methods for detection through testing.
2) perform stress tests to verify failure mechanisms.
3) develop techniques to identify and verify failure mechanisms.

The program will ultimately lead to methods of predicting failure rates through failure mechanism prediction. Furthermore, the study will be essential in developing tests to screen out potentially weak devices after defining specific failure mechanisms as a function of stress level.

The current program is a continuation and expansion of the work started under Contract NASW-973.

## 2.0 SUMMARY

This report covers the effort expended during the second quarter of Contract No. NAS 12-72.

66-32765

The Life test data indicates the devices are exhibiting stable parameter characteristics with exception of the erratic response of the reverse diode leakage current for Vendor A.

The completion of the temperature cycling indicate Vendors B and C appear to have been unaffected, while Vendor A experienced thermo-compression bond failures.

over

2.0 SUMMARY (Cont'd)

The testing of the two new Vendor, D and E, devices has started with the discontinuation of testing Vendor D until problem areas are resolved.

The failure analysis has shown that in addition to purple plaque, imperfections in the dielectric coating have constituted the major source of difficulty. Improvements in the inspection procedure and alternative dielectric coating materials are recommended as a means to both minimize the purple plaque and obtain low leakage current circuits.

AUTHOR

3.0 CONTINUATION OF LIFE TEST

3.1 Vendor A

Vendor A units are continuing life test and will have 5,000 hours completed on 16 March 1966. At the 5,000 hour data point three devices, numbered 9A, 21A and 27A will undergo preliminary failure analysis. Device number 9A has historically been troublesome in nature. Previously, at the 1,000 hour data point, input diode no. 9 showed the classic symptom of inversion channeling. Annealing at 125°C for 24 hours resulted in complete recovery of the diode leakage to approximately its initial value and has remained within the failure criteria. Presently, diode no. 2 has shown an increase in reverse diode leakage from 29.10 nanoamperes initially to 426.7 nanoamperes at the 4,000 hour data point. In both cases the diodes have been under constant reverse bias (4 volts) during the life test and show signs of the same failure mode. However, because of the nature of the problem, the device was returned to test for additional hours and detailed analysis awaits re-evaluation of the data at the 5,000 hour point. It should be noted that even though a device is considered a failure in accordance with the failure criteria established in this study, the actual magnitude of reverse leakage may be within the maximum limits specified by the manufacturer. It is our

3.1 Vendor A (Cont'd)

intent to keep this in mind; however, by maintaining tighter tolerance limits it is hoped that any given failure mechanism may be revealed before it becomes catastrophic in nature.

Devices numbered 21A and 27A are apparent failures. Diode no. 3 of 21A at 4,000 hours has a reverse diode leakage of 61.96 ma and diode no. 3 of unit 27A has a 15.94 μa reverse leakage at 4,000 hours. Special attention will be given to devices 21A and 27Aduring the 5,000 hour data point to determine the validity of the noted failures. In both cases, an apparent softening of the reverse characteristic is occurring as a result of the combined temperature and reverse voltage which is being applied during the test. It might be worthwhile at this time to briefly review the electrical tests during operating life to ensure understanding of the test conditions. The diode at pin 1 is being driven by the signal source (0-4 volts) which in turn switches logic states of one side of the dual gate. Output of gate one is connected to the diode at pin 9 which in turn switches logic states of the second side of the dual gate. All unused diodes (numbered 2, 3 and 8) are connected to a +4 volt supply thus reverse biasing these diodes. The net effect is to study both the active and reverse characteristics of these logic elements.

In a general sense, the data indicates that the remaining devices are exhibiting stable characteristics with the exception of the continued erratic response of reverse diode leakage current. The belief is that mobile ionic contamination is present on or within the oxide or at the Si-$SiO_2$ interface which would cause minor inversion channeling when the devices are subjected to a combination of high temperature and voltage as in the case of the operating life test. The electrical parameter measurements with the exception of the findings already reported show no sign of device degradation which might lead to interconnect, metalization, surface and bulk defects as a result of 4,000 hours of operational life.

3.2 Vendor B and C

Vendors B and C units are continuing life test and will have 5,000 hours completed on 24 February 1966. The 4,000 hour data has been reviewed and the results are contained in the following paragraphs.

Device 19B was reported at the 3,000 hour point as having indicated an increase in output transistor leakage. The measured value of leakage was 492.6 nanoamperes and after annealing at 125° C for 24 hours the reverse leakage returned to near its initial value of 4.8 nanoamperes. Upon completion of an additional 1,000 hours of operating life thes reverse leakage is 22.90 nanoamperes which is within the failure limits. However, because of the original noted failure, device 19B warrants continued observation for the remainder of operational life test. Review of the 4,000 hour data in general, indicates no significant change in electrical parameter characteristics. The significance of these results, is that Vendor B devices are exhibiting stable electrical and metallurgical characteristics, within the detectable limits of measurement accuracy.

Vendor C devices are typically identical in performance characteristics to Vendor B units and also show no significant change in electrical parameter characteristics. This of course, is with the exception of previously noted failures.

4.0 CONTINUATION OF TEMPERATURE CYCLE

4.1 Vendor A

The temperature cycle test has completed the third and final cycle. Results of the test have indicated two device failures. Input diode no. 1 of device 48A indicates an electrical open. Preliminary failure analysis shows a bond failure as the

4.1 Vendor A (Cont'd)

mechanism. A bond separation occurred at the AU-AL interface which is the result of thermal stress induced during test. Initial investigation also indicates the oxide beneath the aluminum has been removed during the separation. The mode of failure is generally accepted as typical; however, detailed failure analysis will be performed.

A second failure has been observed in device number 51A. Input diodes numbered 1 and 2 also failed during the final cycle of temperature cycling. Diode number 1 exhibited a reverse voltage of approximately 8 volts with a reverse current of 1 μa. At 10 μa the reverse voltage increased to a value of approximately 18 volts. The electrical characteristics warranted examination of the device. Preliminary analysis indicated a near open of the thermocompression bond at the aluminum bonding pad. Complete electrical open was easily accomplished with a slight lift of the gold wire. Input diode number 2 on the other hand, shows no apparent bond separation. Electrical measurements indicate simular characteristics as that of diode number 1 but detailed analysis is required to determine the exact mechanism. The only hypothesis which can be generated at this time is that it is also a metallurgical weakness associated with the bond, possible in the form of a crack and/or void.

In a general sense, review of the post environmental data has shown little significant parameter change after 150 cycles of temperature cycling. A significant change based on engineering judgment is defined as shown in Table I.

4.1 Vendor A (Cont'd)

TABLE I

Failure Criteria

| Parameter Type | Significant Change |
|---|---|
| Junction Breakdown Voltage (BV) | ±25% of initial value |
| Reverse Junction Current ($I_R$) | Initial X10 but greater than 10 nanoamperes |
| Saturation Voltage ($VCE_{SAT}$) | ±10% of initial value but greater than 10 millivolts |
| Resistance (R) | ±20% of initial value |

The results of input diode breakdown voltage measurements with the exception of the failures and reverification of erroneous results indicate approximate values of 5 volts which is typical of a gold-doped emitter-base diode as employed in Vendor A devices. The output transistor saturation voltage measurements indicate approximate values of 0.2 to 0.3 volts which also illustrate typical properties of a gold-doped device. The diffused resistors as shown by the data have indicated no significant change in absolute value. Any changes observed can most likely be attributed to instrumentation resolution error and the temperature coefficient of the resistor itself. Reverse leakage current, the most sensitive measurement to device change, has exhibited instability from data point to data point. These changes, however, indicate no detrimental degradation but most likely indicate the existence of minor inversion channeling. Although present, the fact remains, that under the stress conditions of this test, the mechanism is minor. It is important to note that combined with the thermal stress, the devices were reversed biased and the applied voltage of 4 volts is typical of the logic levels encountered in actual application. The net result of the reviewed data at this time shows:

1) Potential bond weaknesses as witnessed by two device failures.

4.1 Vendor A (Cont'd)

2) Minor inversion channeling but of little or no concern.

It should be noted that additional investigation is presently being conducted on the remaining final measurements taken at the completion of the temperature cycling test. However, the results of the post environmental measurements (repeated measurements) would indicate no significant findings in regard to additional potential problem areas.

4.2 Vendors B and C

Results of the temperature cycle test, upon completion of the third and final cycle shows little change in parameter values. Vendors B and C devices have exhibited extremely stable characteristics during the applied thermal and voltage stresses. The significance of these results are that Vendors B and C devices for all practical purposes are unaffected by the temperature extremes and reverse bias voltages of this test. The breakdown voltage characteristics indicate no input diode defects, and associated thermocompression bond or interconnect problems. Reverse leakage has revealed in a broad sense no passivated surface and inversion channeling difficulties. The saturation voltage characteristics of the output transistor from a practical-device point of view has shown no degradation in it's active characteristics. This in turn provides a relative measure of DC gain stability and in addition, indicates no degradation in the offset diodes. In a metallurgical sense no interconnect or bonding problems were uncovered. The resistance measurements indicated no degradation as expected. It should be pointed out again that only the post environmental measurements as previously noted were scrutinized. However, from the data analyzed to date no significant findings in regard to potential problem areas is anticipated.

## 5.0 CONTINUATION OF TEMPERATURE STRESS TEST

### 5.1 Vendor A and C

Temperature stress testing has been resumed and step 6 (330° C) has been completed. The collected data has not completed data processing and, therefore, a comprehensive review of data has not been performed. The newly employed data processing technique requires the transfer of all initial data from data sheets onto IBM cards. All environmental data is compared with the initial data which makes the transfer required prior to processing. Expected completion of the reduced data is 25 February 1966. However, from general inspection little change has occurred between step 5 (315° C) and step 6 (330° C). There is still continued evidence of junction softening as indicated by an increase in reverse leakage current. The output transistor saturation voltages on the units also show degradation which is to be expected due to the formation of intermetallic compound beneath the gold-aluminum bonds at the chip.

Since, the temperature stress test has once again been resumed, additional effort is presently being initiated and expected completion of the temperature stress test is 11 March 1966.

## 6.0 STUDY OF NEW DEVICES

### 6.1 Vendor D

The devices in the circuit form of "complementary transistor logic", (DTL) were received in January. The circuits are a five input "AND" or "OR" GATE with an NPN emitter follower output. The input gate is made up of five PNP transistors having common collector and emitter connections.

The package construction with Kovar plates is as described in the 30 November 1965 Quarterly Report.

6.1 Vendor D (Cont'd)

During the initial measurements nineteen devices were catastrophic failures. Each device had a combination of failure modes. The basic failure modes were:

1) base-emitter shorts on the input transistors
2) collector-base shorts on the input transistors
3) collector-emitter shorts on the input transistors
4) collector to substrate near shorts on the output transistor

Testing was discontinued on Vendor D devices until the problem areas are resolved. The manufacturer was notified and copies of the test procedure and data were sent to him. Also, two devices with serial numbers 53 and 60 were sent to Manufacturer D for analysis of the fabrication processes.

We were subsequently notified that devices with the external leads bonded directly to the aluminum bonding areas on the chip are no longer available because the development was discontinued.

6.2 Vendor E

Vendor E devices have started test. Group II, samples numbered 6 through 25 have completed 100 hours of operating life. Results of the first 100 hours of operational life show no device failures and very little change in parameter characteristics. The units have been placed back into test and expected completion of the 250 hour measurement interval is 28 February 1966.

In addition, the temperature cycle test has begun and the first 50 cycles will be completed on 25 February 1966, at which time measurements will be performed.

Temperature stress testing awaits completion of the temperature cycle test.

6.2 Vendor E (Cont'd)

In general, results of the initial measurements and environmental measurements obtained to date indicate stable device performance and no early device problems have been noted.

## 7.0 FAILURE ANALYSIS

### 7.1 Status of Failure Investigations

The devices which have been investigated and the major source of failure are summarized in Table II.

TABLE II

Summary of Investigated Devices

| Device No. | Defect |
|---|---|
| 88B, 69B, 73B and 80B | Purple Plague |
| 75A, 100A, 43A | Dielectric Imperfection |
| 31C | Tubular Imperfection in Silicon |

### 7.2 Purple Plague

The purple and black plague, the formation of various aluminum-gold alloys, have been discussed at some length at a recent symposium*. It was postulated that the plague can be attributed to diffusion of gold into the aluminum. Recent studies** on circuits purchased from Manufacturer II have revealed the presence of purple plague when the bond is directly in contact with the silicon die and the absence of the plague when the protective dielectric layer was interposed between the silicon and the electrode connection. It is apparent therefore, that under certain conditions a passivating surface can provide some protection.

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* Browning, "Failure Mechanisms Associated with Thermocompression Bonds in Integrated Circuits", Physics of Failure in Electronics 4th Annual Symposium, November 1965.

** Company IR and D Sponsored: Roman Numerial designations are used when device studies were performed through Company funding.

7.2 Purple Plague (Cont'd)

Manufacturer II's device had only been subjected to an 85° C environment when the failure occurred. The device of Manufacturer B had developed purple plague after being exposed to 250° C. It is possible therefore, that the passivating surface protection is only partial and the distinction between direct bonding with silicon and bonding on a passivated area would disappear at higher temperatures. An attempt is being made to obtain a second device from Manufacturer II and subject it to a higher temperature environment to investigate this possibility. This investigation will be completed during this next quarter.

To investigate the possibility that the dielectric of Manufacturer II may actually be a better protector than the dielectric of device 80B, a detailed study was made of the two dielectrics. The results are summarized in Table III and discussed below.

TABLE III

Comparison of Dielectric Properties of Two Devices

| Part | Thickness | Etch Rate |
|---|---|---|
| Device 80B | 10,000A° | 2A°/sec |
| Manufacturer II - 3011 | | |
| lower layer | 4,200 | 4A°/sec |
| upper layer | 6,600 | 50A°/sec |

a) Device 80B

Device 80B had been subjected to several temperature step stress tests up to 250° C. All of the gold thermocompressed bonds had blackened at the thin film aluminum interface; the set of bonds which were in direct contact with the silicon, and the set of bonds which were separated from the silicon by $SiO_2$ passivating layer.

7.2 Purple Plague (Cont'd)

The aluminum electrodes were chemically removed with concentrated hydrofluoric acid. Further treatment with aqua regia was required to remove pure gold and some partially oxidized and silicated aluminum which apparently formed during the elevated temperature treatment. Additional treatment with potassium tri-iodide was required to remove the black intermetallic compound which had formed. The underlying $SiO_2$ layer was found to be macroscopically perfect.

The $SiO_2$ layer was removed chemically. The etch rate was 2A°/sec which indicates a dense thermally grown oxide. There was no difference between the $SiO_2$ which was directly under the bond and the remaining part of the $SiO_2$ layer. Thus, one might conclude that Browning's mechanism is completely valid.

b) Device 3011 (Manufacturer II)

The passivating layer of device 3011 is made up of two different dielectric layers. The upper layer is very reactive to dilute hydrofluoric acid dissolving at the rate of 50 to 60 A°/sec. The lower layer is much less reactive dissolving at the rate of 4 to 5A°/sec.

In addition to the difference in reactivity of the two layers, it was noted that the aluminum interacted much more extensively with the dielectric than the aluminum dielectric interaction of Device 80B. Further experimentation appears warranted to determine whether or not there is a marked difference in the capabilities of the two dielectric materials to prevent purple plague.

## 7.3 Dielectric Imperfections

As indicated in Table II, dielectric imperfections have been noted in devices 75A, 100A, and 43A.

Over and above the fact that the coincidence of imperfect dielectric coatings in the region of failed devices, is cause for concern about the dielectric structure, it should be noted that dielectric imperfections are obvious in sections of the circuit which have not yet failed.

It is recommended that NASA request pictures of microcircuits just prior to aluminization in order to assess the uniformity of the dielectric coatings. A 250 magnification should be sufficient to indicate whether or not the various manufacturers have their dielectric process under control.

For completeness, the history and status of each device is given below:

### Device 75A

A small defect was noted crossing over the junction from the N+ to the P region. The dielectric was removed completely and the defect remained on the silicon surface. Whether the defect was in the silicon originally, or whether migration along the dielectric defect induced the irreversible defect could not be proved.

Copper staining was performed to determine whether or not the junction region was primarily N+ or P. Inconsistencies in the staining prevented this determination but the inconsistencies confirm the probability of surface contamination possibly through inversion layer formation.

The device was etched for one minute with a weak etch consisting of 1 part HF, 3 parts $HNO_3$ and 8 parts acetic acid. The original

7.3 Dielectric Imperfections (Cont'd)

defect disappeared with this treatment confirming the fact that the defect did not penetrate deeply into the bulk silicon.

Device 100A

The source of this failure was reported on at length in the June 1965 monthly progress report.

There it was shown that there was a flaw in the dielectric extending from the N+ region to the P-N junction.

This device was reconstituted in the sense that replacement of the oxide and thin electrode film connection showed that the non-leaky diode remained non-leaky while the leakage of the defective diode was only partially reduced.

Again it is impossible to positively state that the silicon was originally perfect and the failure was caused by the imperfection in the dielectric providing a path for migration of aluminum to the silicon, but the probability is there.

An attempt was made to prove the existence of a unique doping in the silicon corresponding to the imperfect dielectric region. The new oxide was removed and the device stained.

Again, as in device 75A, there were inconsistencies in the staining and it was impossible to prove the existence of a unique doping in the position corresponding to the dielectric.

Device 43A

This device had a defect in the dielectric which extended to a depth of only 45° A below the dielectric upper surface. Approximately 700A° remain over the silicon region. Thin film electrodes were redeposited and the original leakage disappeared.

7.3 Dielectric Imperfections (Cont'd)

This device is being forwarded to NASA as instructed.

7.4 Possible Silicon Imperfection

The only case in which a possible defective silicon wafer was used has been uncovered in the investigation of Device 31C.

On investigation of the circuit, even prior to aluminum removal, a defect was clearly discernible extending from the anode to the cathode of diode No. 7. The defect is clearly discernible even at 100 magnification; Figure 1.

A 1070 magnification view is shown in Figure 2 after the oxide removal. The defect clearly extends into the silicon.

In order to study this defect further, the device was angle lapped and etched. The section was taken at 10 degrees perpendicular to the direction of the defect. Figure 3 is a 950 magnification view of the sectioned device, while Figure 4 is a schematic of the view.

Close scrutiny of the device both prior and subsequent to angle sectioning leads to the following conclusion. The defects are tubular in nature both "tubes" having a diameter less than 0.0001 inch. One of the defects was barely visible from the surface view, but was clearly evident from the sectioned view.

It is difficult to imagine that the defects were visible on the surface during fabrication. Rather, it is probable that during the step stress test the thin covering of silicon cracked revealing the "tubes" beneath the surface.

Pictures of the defect are being forwarded to the supplier to determine whether or not they can confirm the existence of such tubular defects in bulk silicon.

## 7.5 Analysis Study on New Devices

Two devices from Vendor D, serial numbers 36 and 57, were used to become familiar with the construction and to develop techniques for disassembling of the device package.

The microcircuits were packaged in a fritted glass sandwich type of assembly between two gold plated kovar platelets. Two platelets were not parallel to each other in either package. The dimensions of the silicon chips were 0.007 inches by 0.009 inches.

Device 36D was opened by lapping along the edges. This technique proved to be an undesirable approach as the device cracked open during lapping and the chip was recovered in five pieces. Although the autopsy technique was not a complete success, examination of the device was achieved. Investigation indicates N-P-N transistors and P-N-P transistors on the same monolithic wafer with no apparent isolation. The input P-N-P transistors are formed by utilizing the base, collector and substrate areas.

Angle lapping two of the input transistors confirmed a two step diffusion cycle; an N type diffusion in the P substrate for the base, and a P type diffusion in the N base region for the emitter. The grounded P type substrate (pin no. 8) functioned as the common collector for all of the input transistors.

A different approach was used to open device 57D. The package was first molded in lucite and then lapped on emery cloth to remove the kovar platelets and glass material over the surface of the silicon chip. During the lapping external leads broke loose from the bonding areas on the chip which broke away chunks of silicon. Mechanical means were tried to remove the fritted, but this caused more silicon to break off. Organic solvent was used in an attempt to dissolve the organic binders, but proved not to be successful. Nitric acid was then tried which reacted with the fritted glass. This reaction would incidate that the glass is a lead compound.

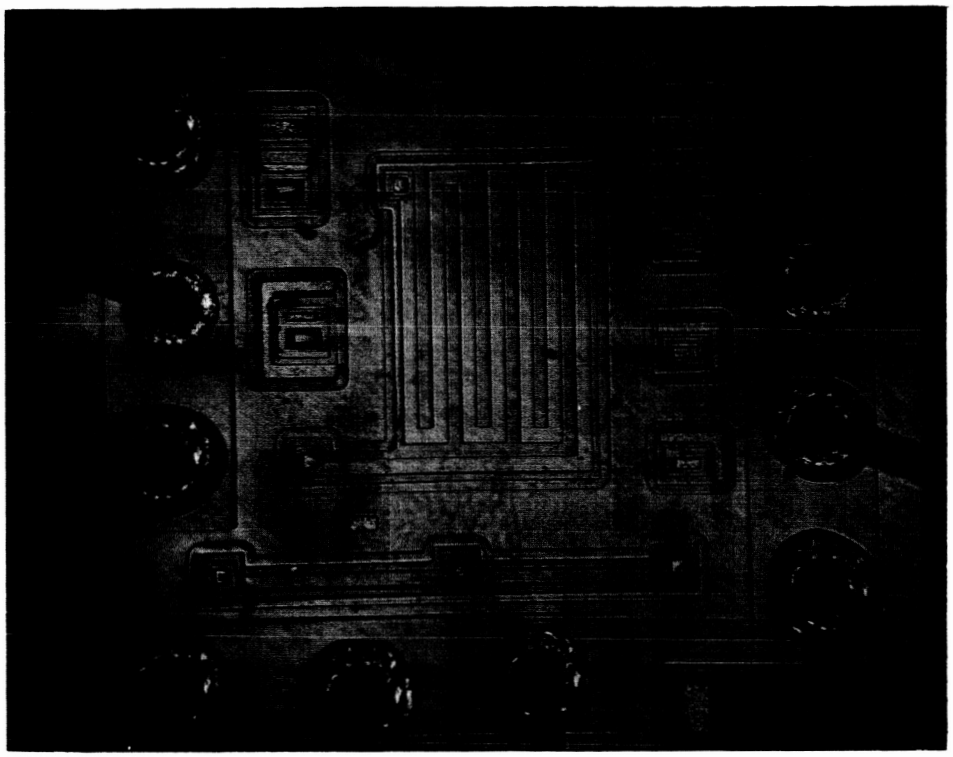

Figure 1
100 × Magnification Device 31C After
Removal of Al Metallization

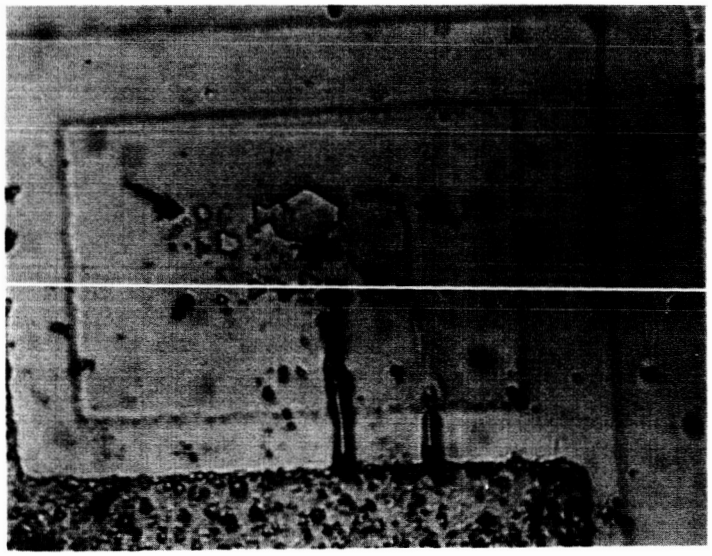

Figure 2
1070 × Magnification Diode No. 7. Defects
Bridging the Anode to the Cathode

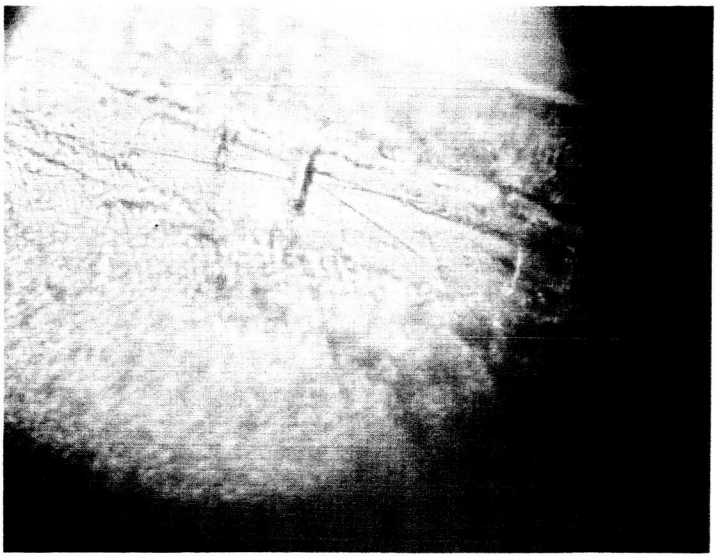

Figure 3
950 × Magnification Diode No. 7.
10° Angle Sectioning of Defects

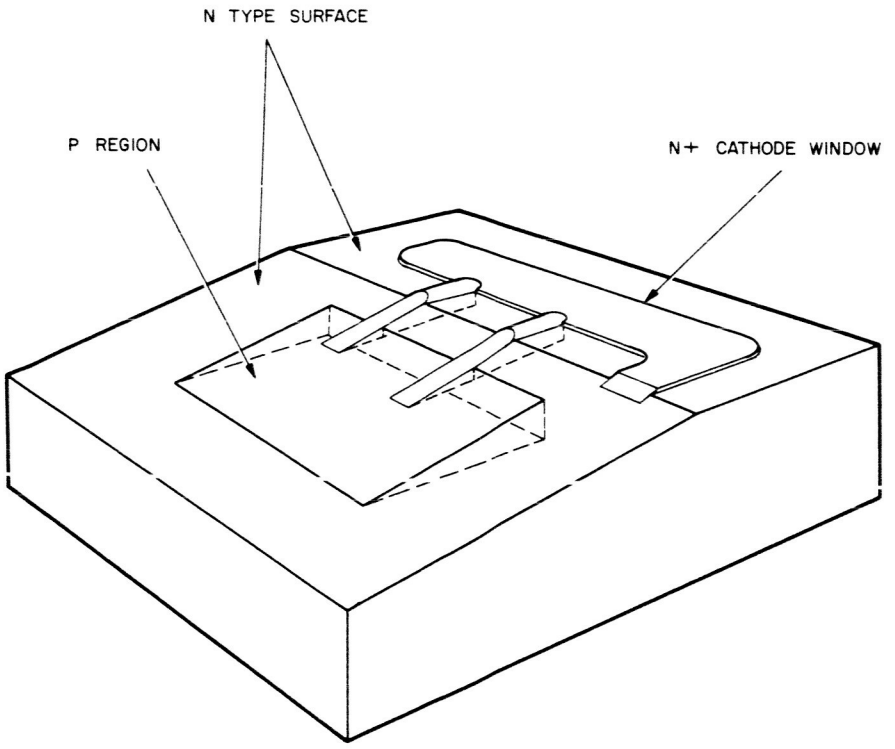


Figure 4
Schematic Drawing of 10° Angle
Sectioning in Figure 3

7.5 Analysis Study on New Devices (Cont'd)

Aqua Regia was used to remove the aluminum metallization. The aluminum metallization had left discolored imprints on the oxide surface, indicating interaction between the aluminum and the oxide. It was also noted that the oxide over the input transistors numbers 1, 4 and 5 was damaged, possibly due to interaction with fritted glass. The damaged oxide may have failed to protect the transistors electrically.

In both devices 36D and 57D the aluminum metallization was discolored even before packaging as indicated on the vendor supplied photographs.

Texas Instruments SN532, "AND or "OR" GATE is shown on the manufacturer's specification sheet to be interchangeable with Vendor D's "AND" or "OR" GATE and was used for verification of the instrumentation. The package for the SN532 is a metal flat pack 1/4 inch by 1/8 inch.

The top of the SN532 device was removed and the microcircuit was examined for comparison with Vendor D's devices.

The dimensions of the silicon chip was 0.007 inches by 0.015 inches. The chip was glued to a ceramic base with a clear plastic. All of the transistors were isolated from the substrate. The aluminum metallization was bright without discoloration due to oxide formation. No further analysis will be performed on this device.

The results obtained from experimentation with the Vendor D package, even though not completely perfected, has led to belief of success in future attempts. The steps will be accomplished by (1) removing the kovar platelets by lapping, and (2) removing the glass frit with $HNO_3$ etch.

## 8.0 Data Reduction Program

To facilitate data reduction, electronic data processing programs have been developed and checked out which will speed up the reduction of the increasing amount of data.

The data is entered on standard 80 column IBM punch cards. The IBM cards are processed through the computer which is programmed to statistically reduce the data. The statistical information is presented onto two sheets; one sheet contains the computed statistics and the other statistical data.

The computed statistics sheets contain a listing of the initial data and post environmental data. In addition, the difference (initial reading - post environmental reading) and percent change from the initial of each device is computed.

The statistical data sheets contain the percentiles, initial group mean, post environmental group mean, mean difference, number of temporary failures and number of catastrophic failures. A catastrophic failure is defined, for the purpose of this program, as a failed device which has been removed from test and subjected to detailed failure analysis. A temporary failure is defined as a device which has reached the failure limits on one or more parameters but is under going preliminary failure analysis or placed back into test for further investigation.